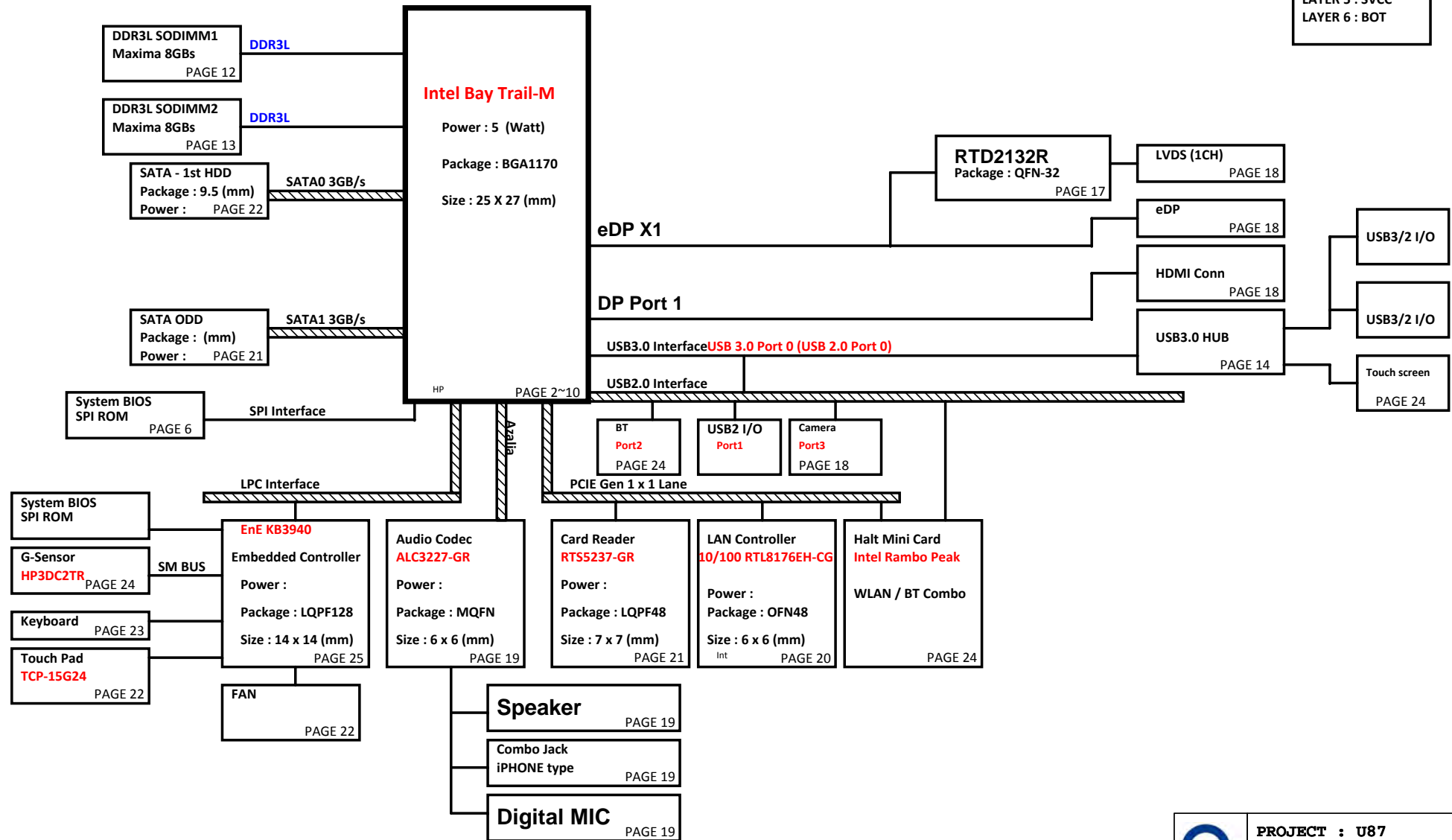
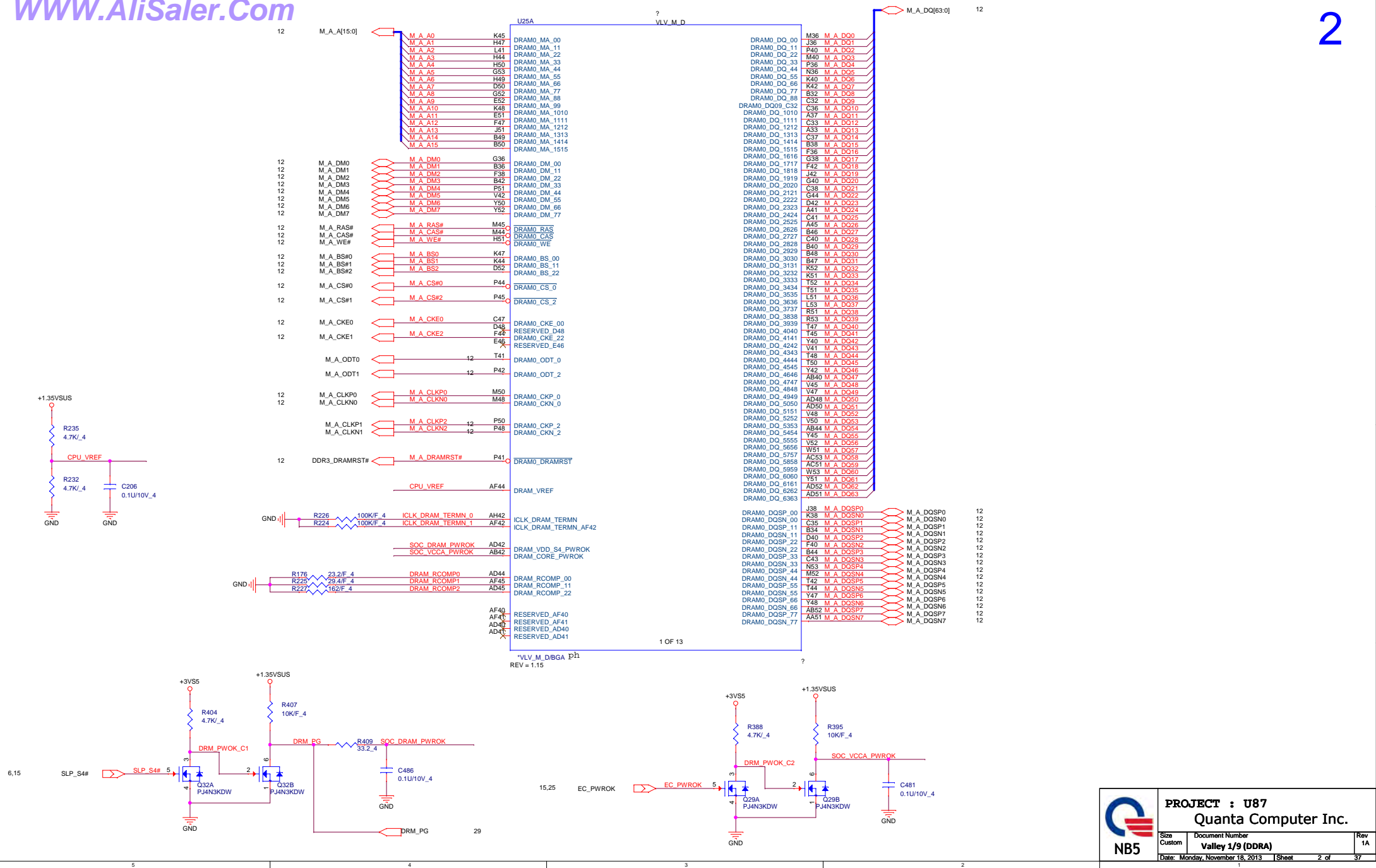


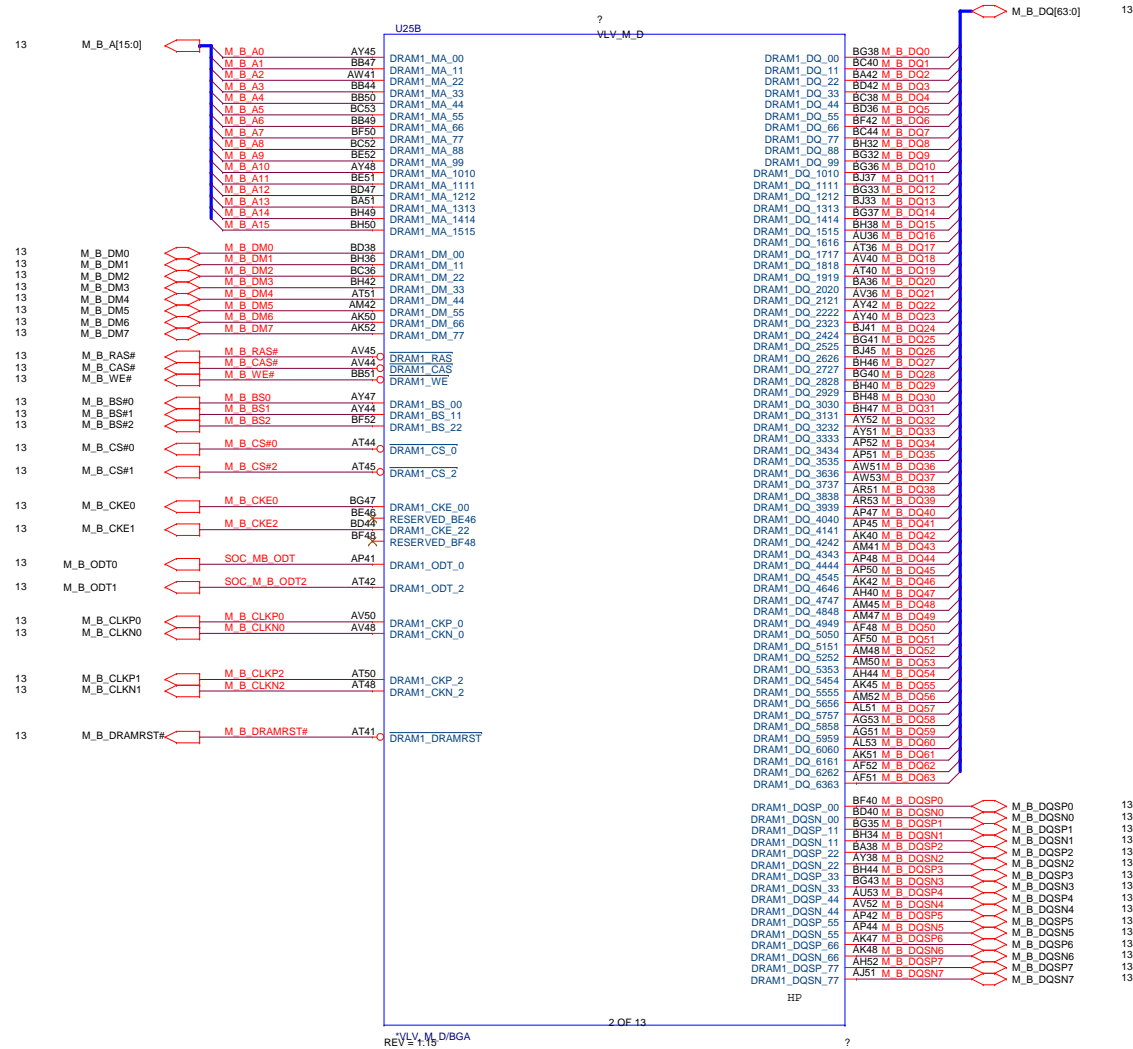
U87/U88 UMA (14"/15.6") Ultra/Slim Intel Bay trail-M Platform Block Diagram

PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT

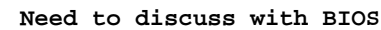




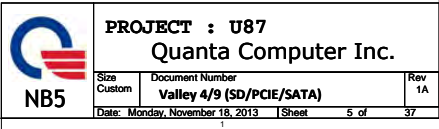


PROJECT : U87
Quanta Computer Inc.

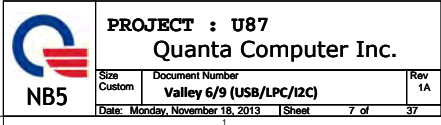
Size	Document Number	Rev
Custom	Valley 2/9 (DDR8)	1A
Date: Monday, November 18, 2013		Sheet 3 of 37

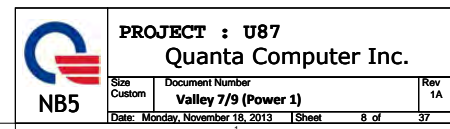


GPIO26	0	0	
GPIO25	0	0	0=HDD+ODD, 1= eMMC only
GPIO24	0	1	0=14", 1=15"

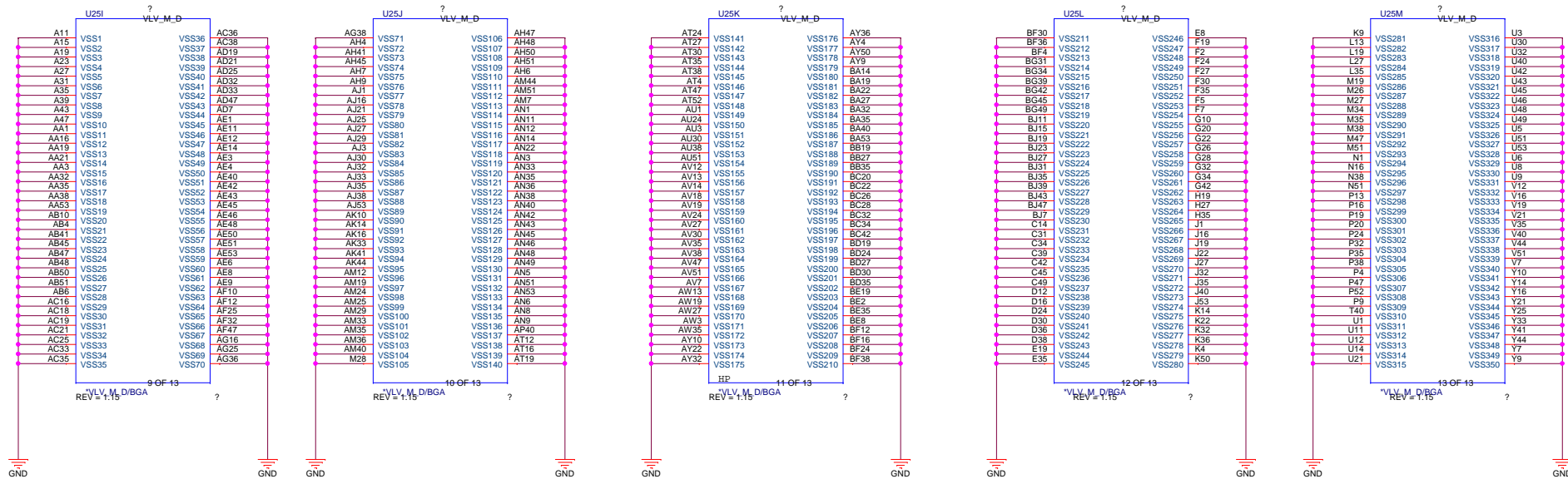


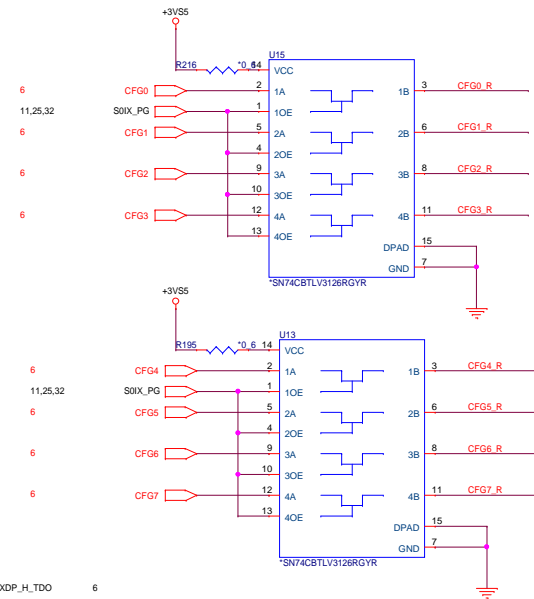







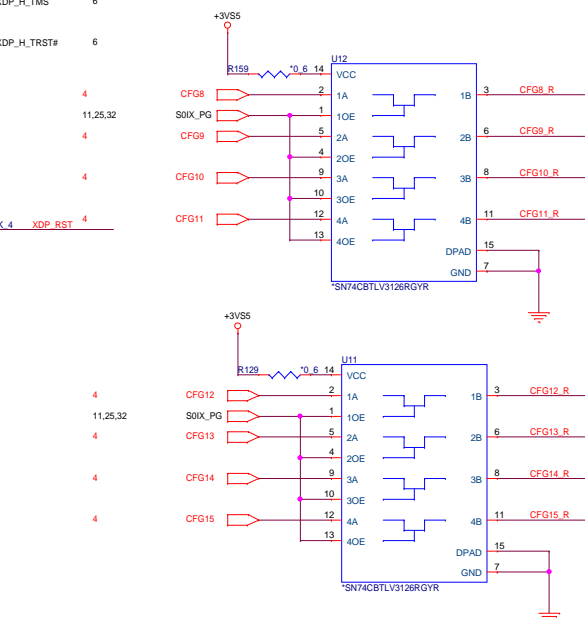


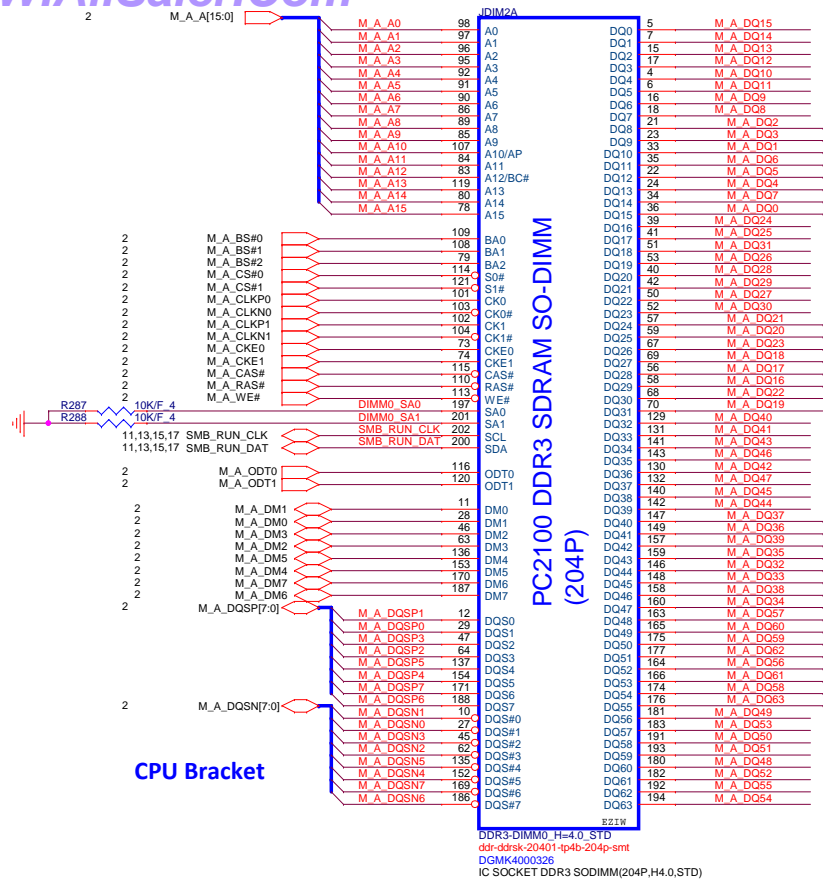




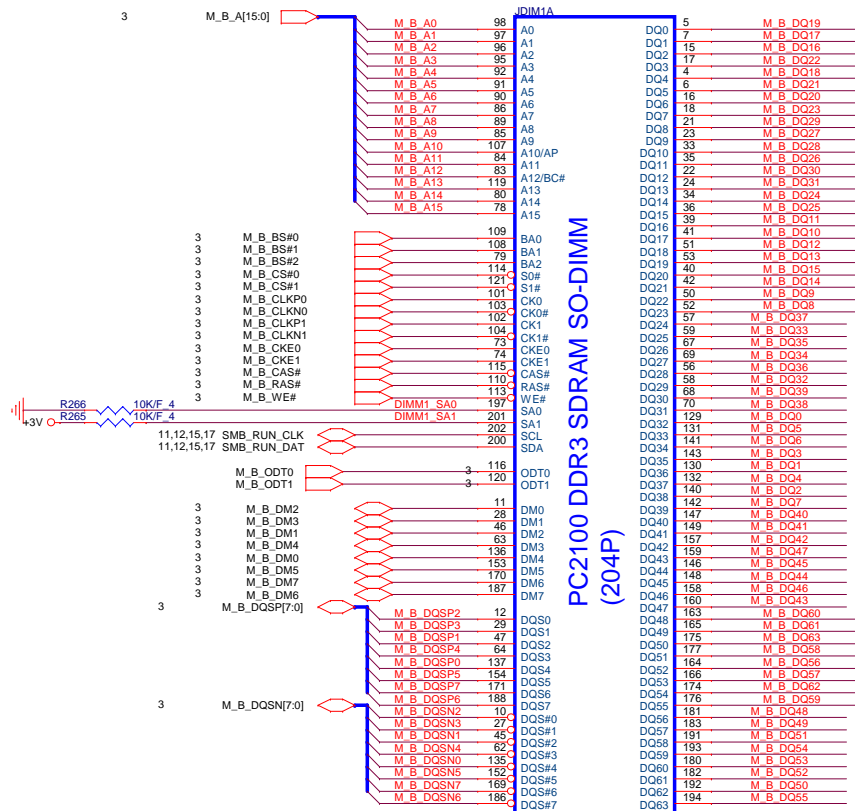


The diagram shows four horizontal signal lines: XDP_TDO, XDP_TDI, XDP_TMS, and XDP_TRST#. Each line has a red arrow pointing to the right, indicating a signal transition or timing point. The labels XDP_H_TDO, XDP_H_TDI, XDP_H_TMS, and XDP_H_TRST# are positioned to the right of the arrows.

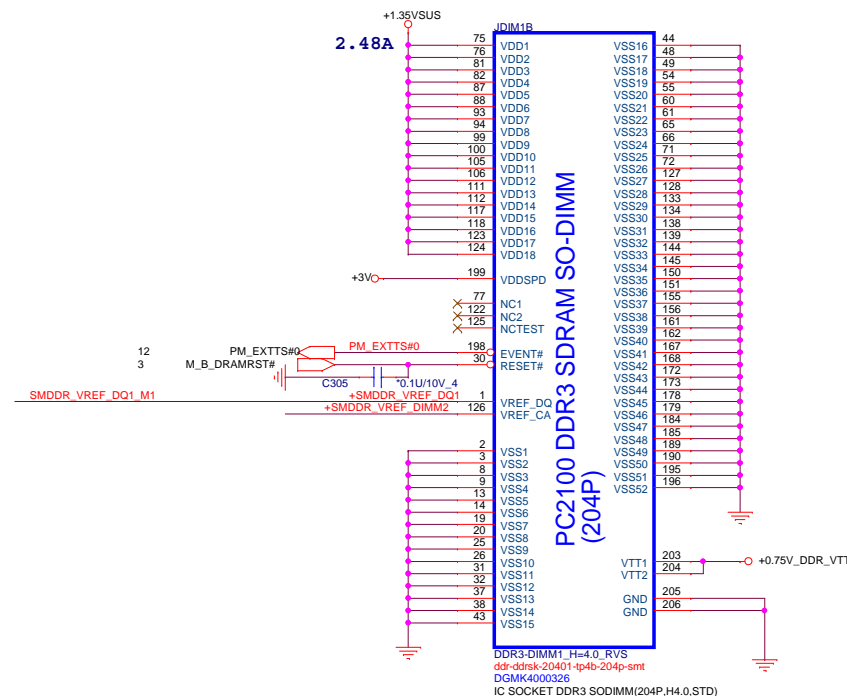


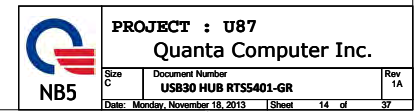


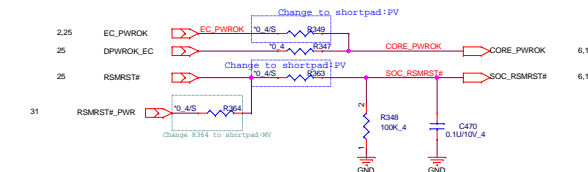
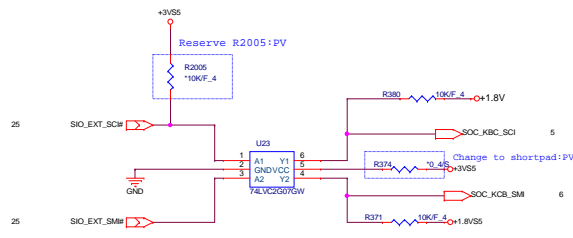
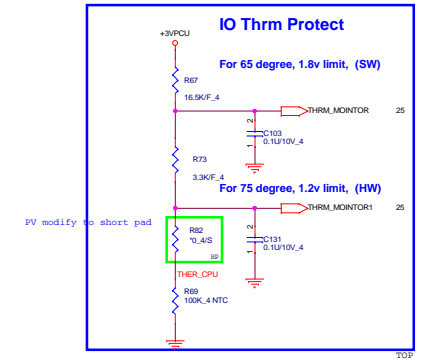
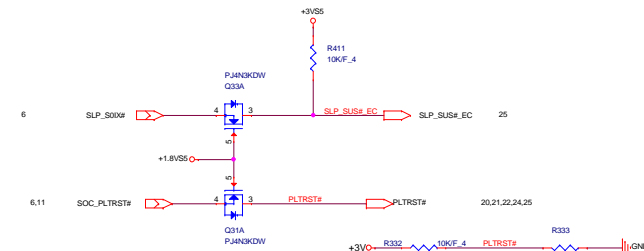
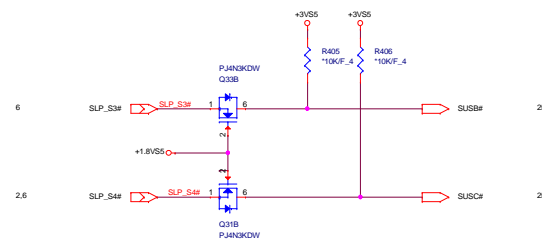
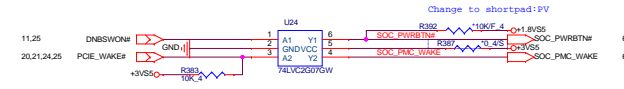
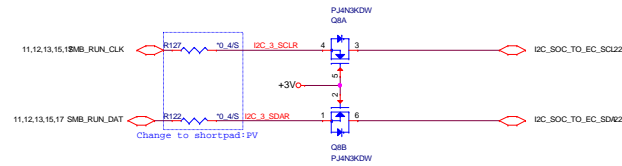
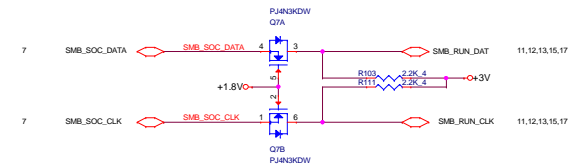
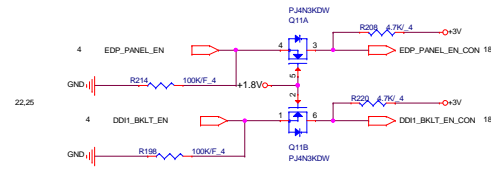
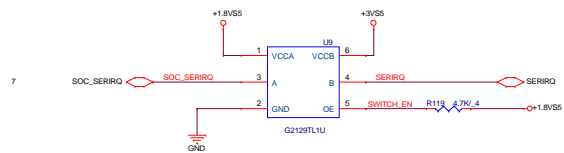
M_B_DQ[63:0]



DDR3-DIMM1_H=4.0_RVS
ddr-ddrsk-20401-tp4b-204p-smt
DGMK4000326
IC SOCKET DDR3 SODIMM(204P,H4.0,STD)







NB5	PROJECT : U87		
	Quanta Computer Inc.		
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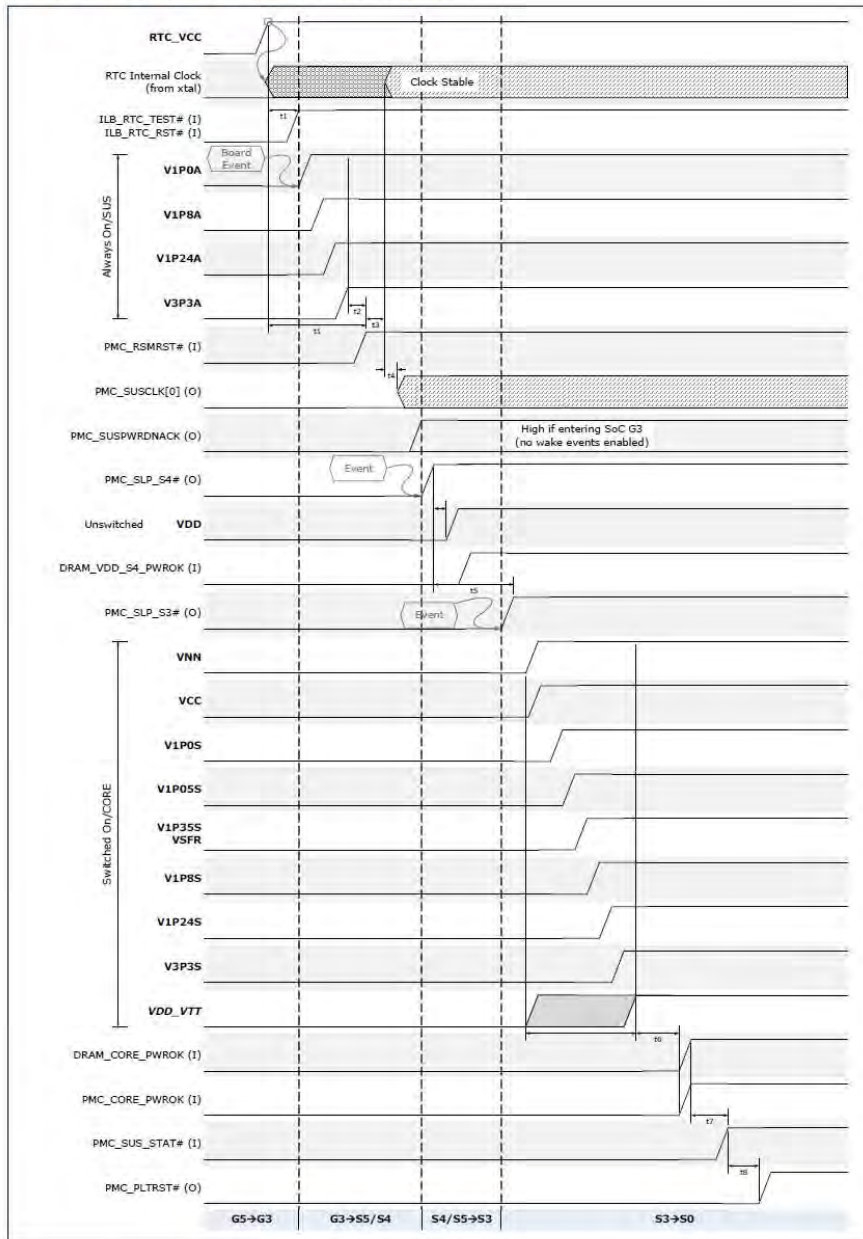
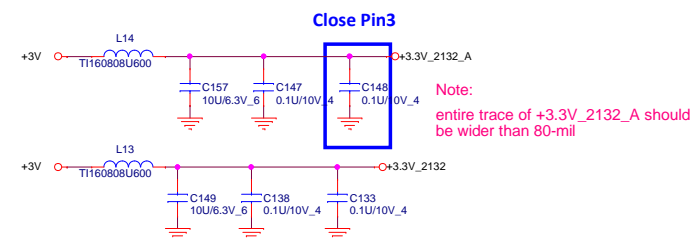
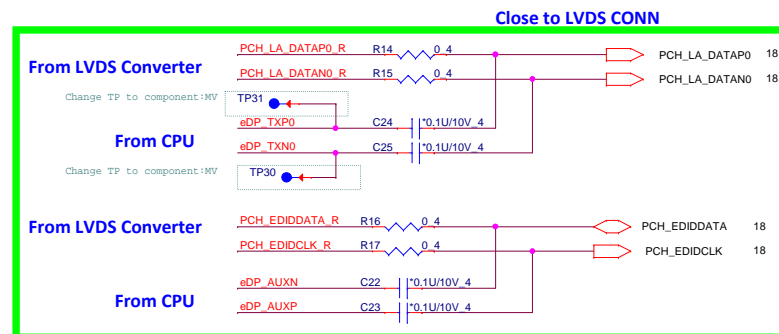


Table 4-12. Cold Boot Timing Spec

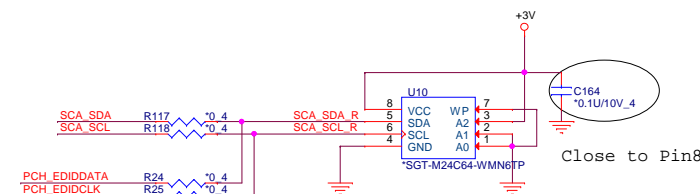
Parameter	Description	Min	Typ	Max	Units
T0	RTC_VCC stable to ILB_RTC_TEST# high	9			ms
T1	VR ramp up time from 10% to 90% voltage level			2	ms
T2	Rail to subsequent rail turn on delay	10		2000	us
T3	VSUS stable to PMC_RSMRST# high	10			ms
T4	S and SX rails stable to PMC_CORE_PWROK	100			ms

NOTES:

1. T1 and T2 are recommended time for all the VR rails unless specified otherwise. The VR ramp up time T2 and subsequent rail delay T3 are put in place to avoid inrush current which may be caused by multiple loads turning on simultaneously or fast charging of VR output decoupling.
2. Violation of rail-to-rail sequencing may cause the SoC part long term reliability issue.
3. Platform devices other than SoC sequencing are not explicitly shown as they are not limited by the SoC sequencing requirement.



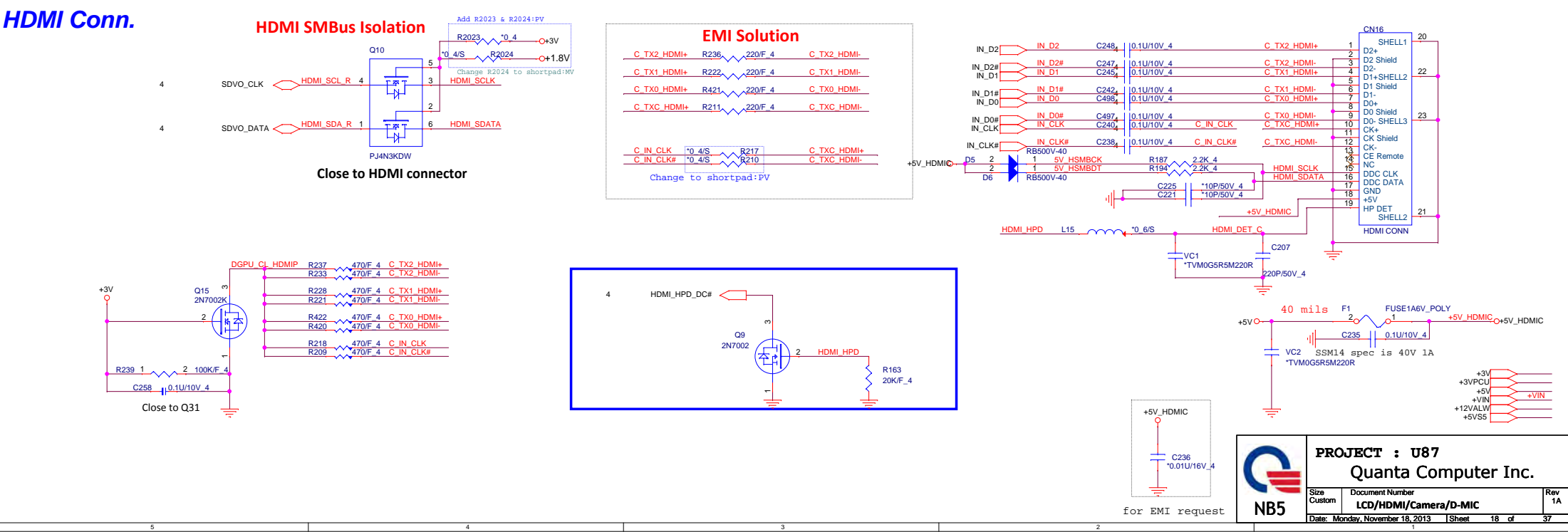
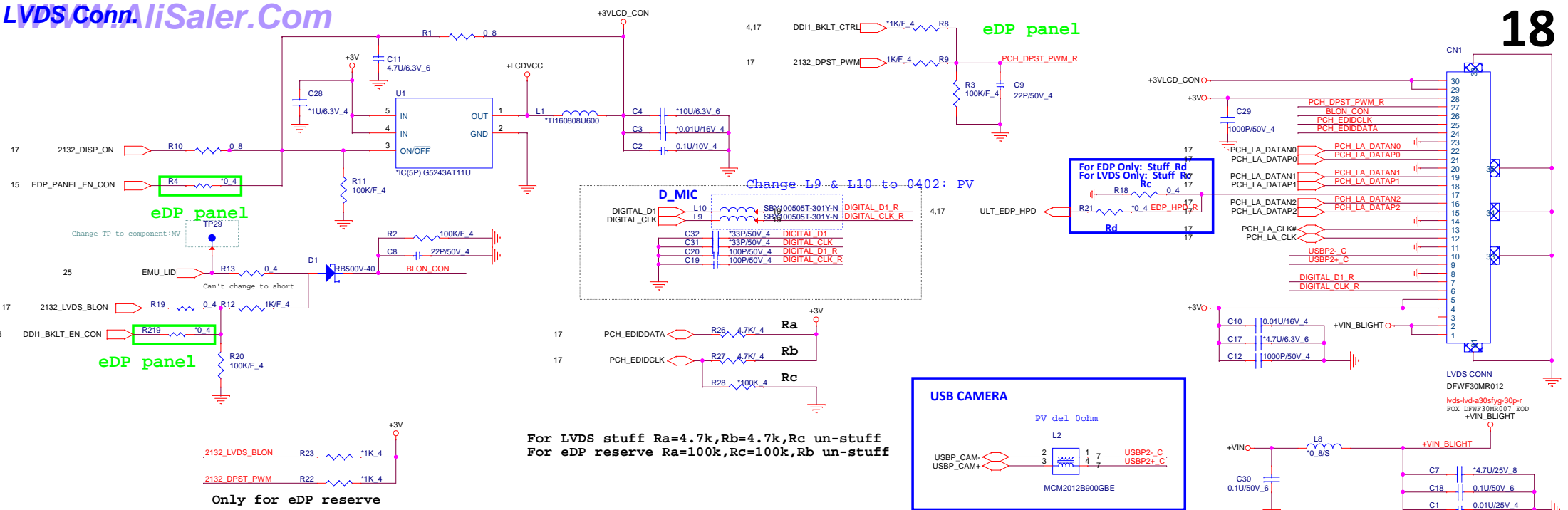
Address=0xA8




		MODE_CFG0(PIN30)	
		0	1
MODE_CFG1(PIN31)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE



Size Custom	Document Number LVDS converter RTD2132R	Rev 1A
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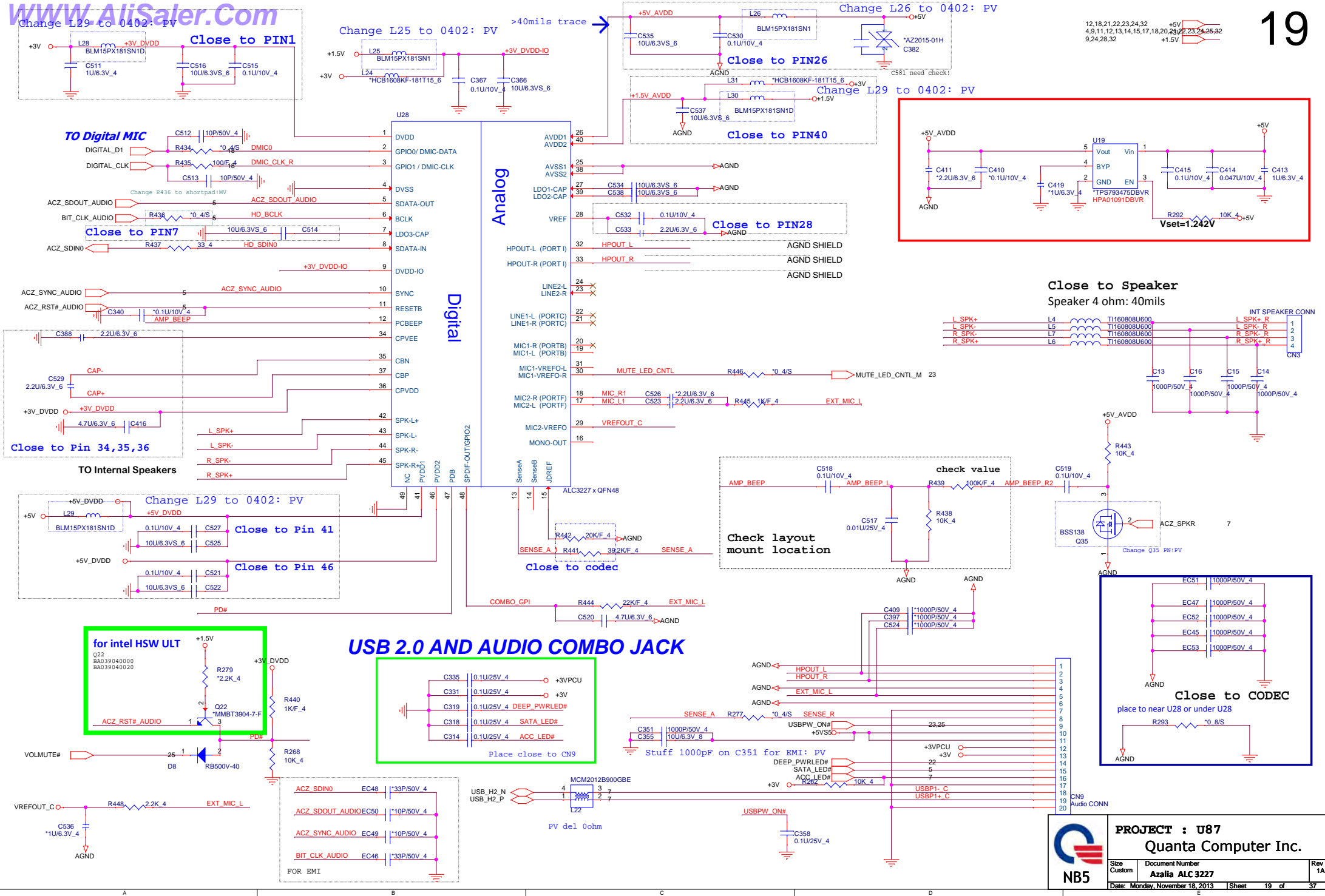


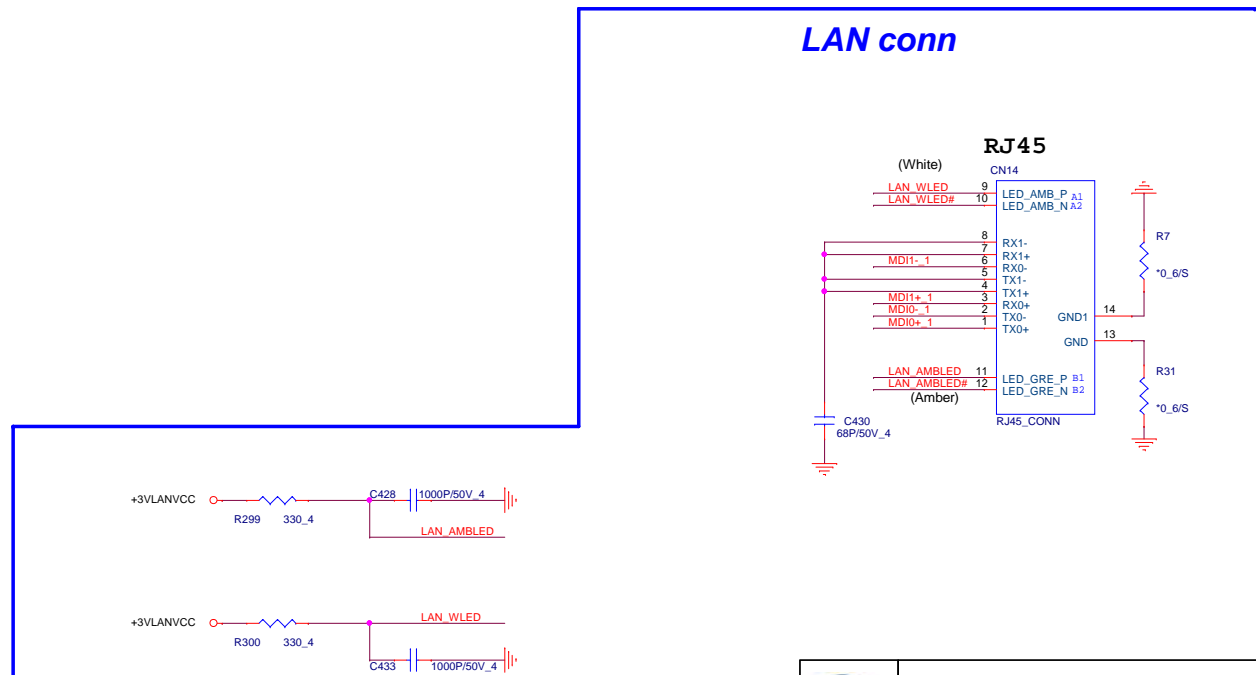
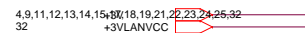
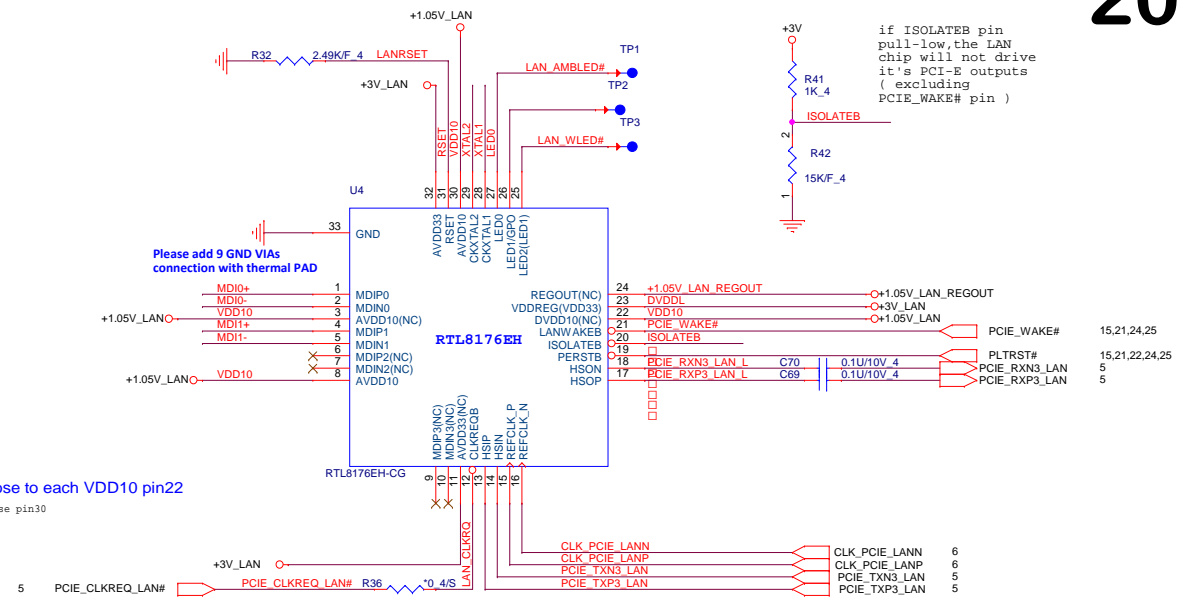


PROJECT : U87
Quanta Computer Inc.

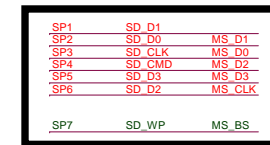
Size	Document Number	Rev
Custom	LCD/HDMI/Camera/D-MIC	1A

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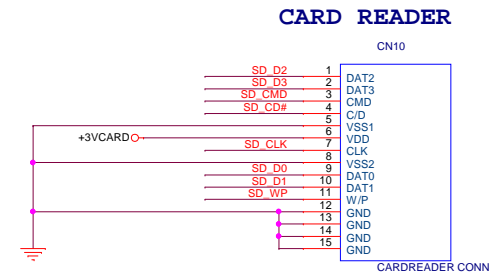





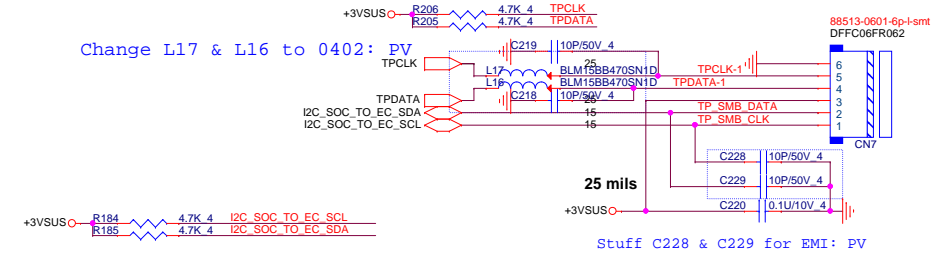
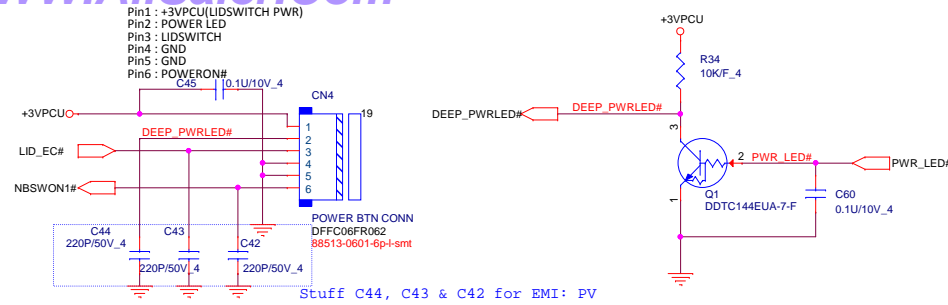
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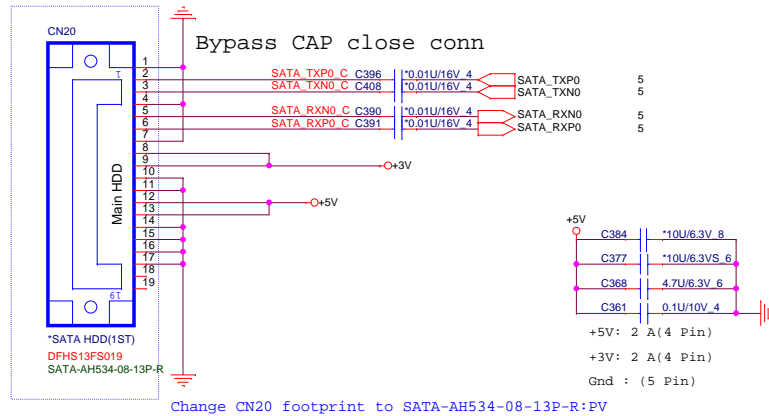
SD / MMC



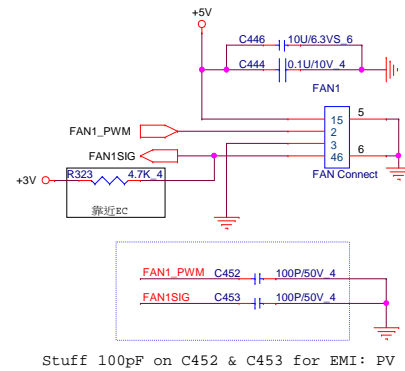
	PROJECT : U87 Quanta Computer Inc.		
	Size Custom	Document Number CR RTS5237 & CR SOCKET	Rev 1A
	Date: Tuesday, April 15, 2014	Sheet 21 of	37



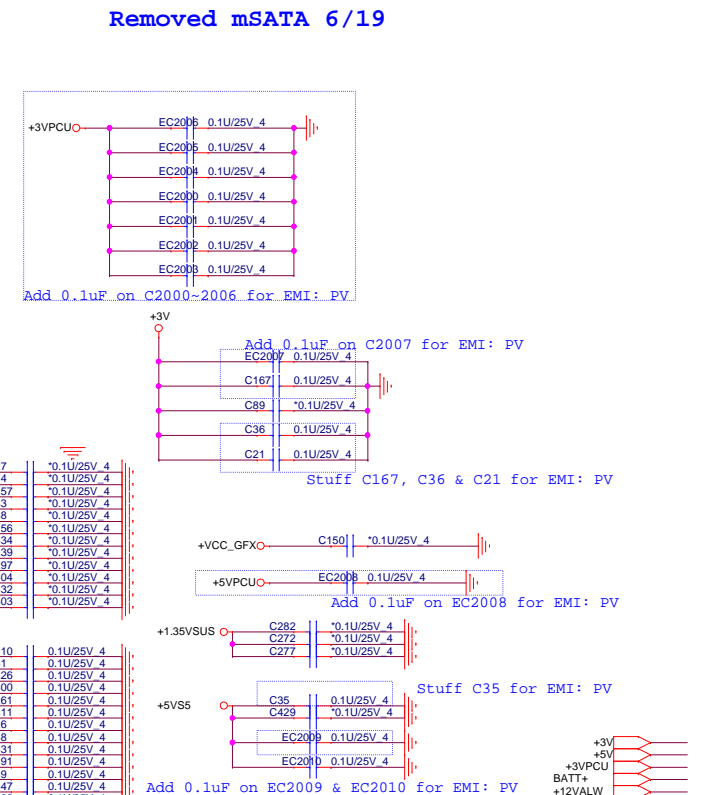
SATA HDD Connector(Cable type)



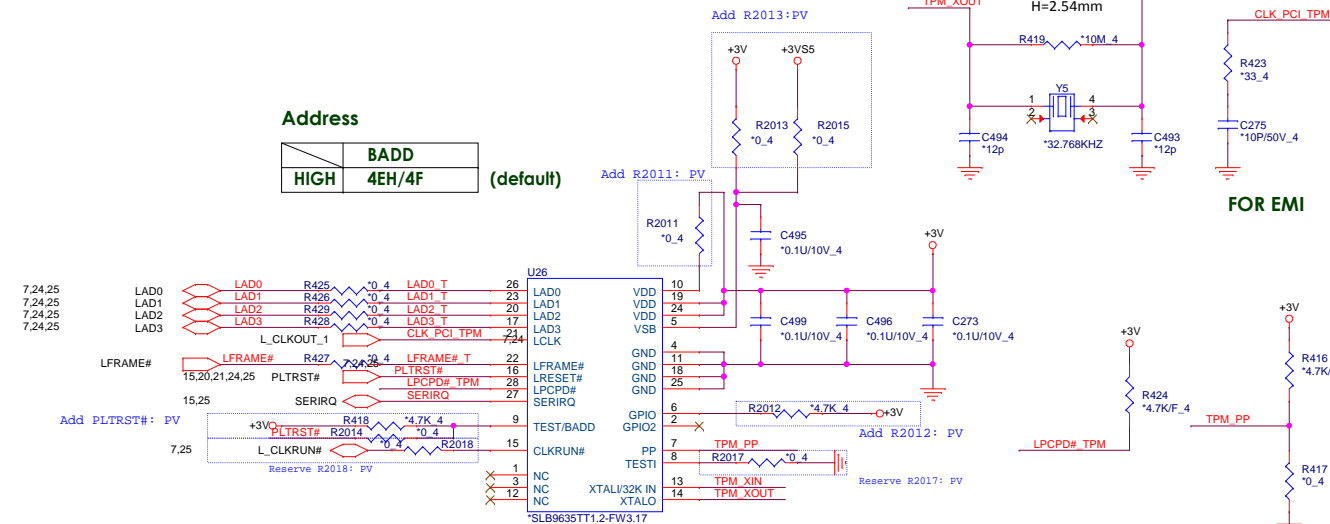
FAN



Mini PCI-E Card 2- Full size mSATA



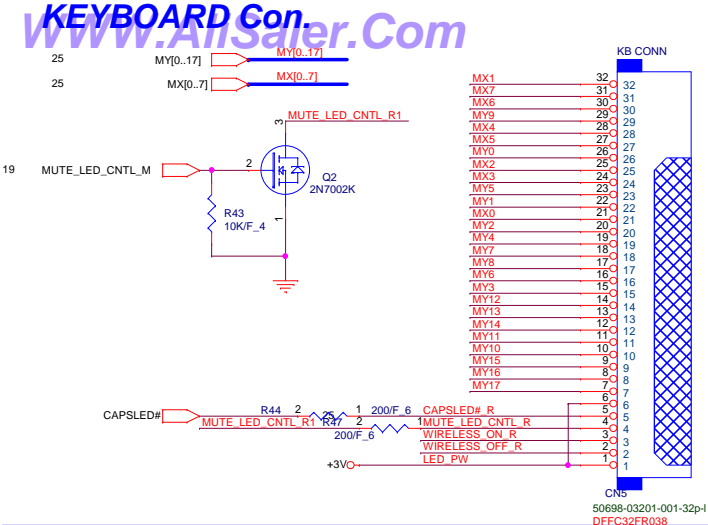
TPM (1.2)



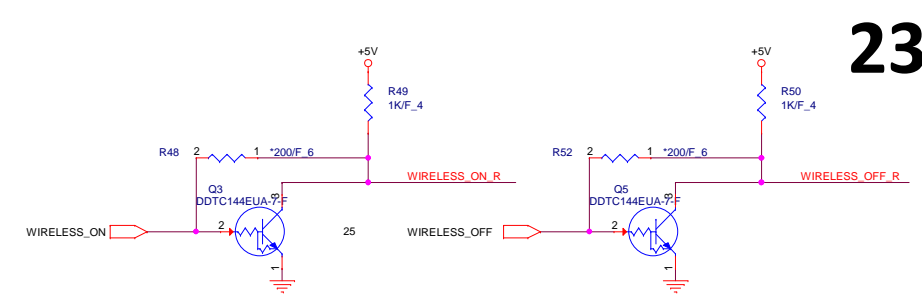
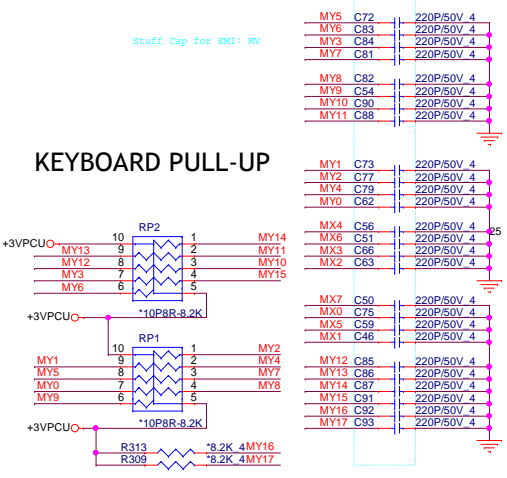
PROJECT : U87

Quanta Computer Inc.

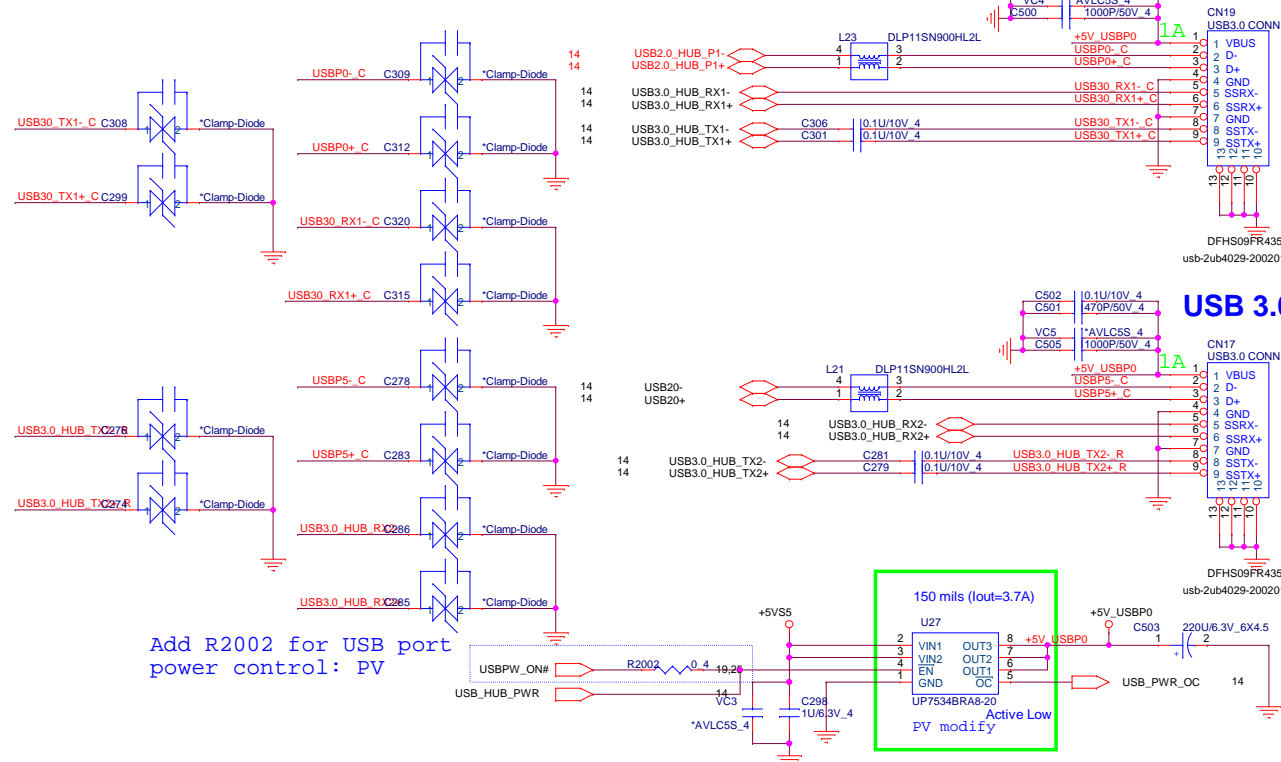
Size Custom	Document Number HDD/mSATA/FAN/LED	Rev 1A
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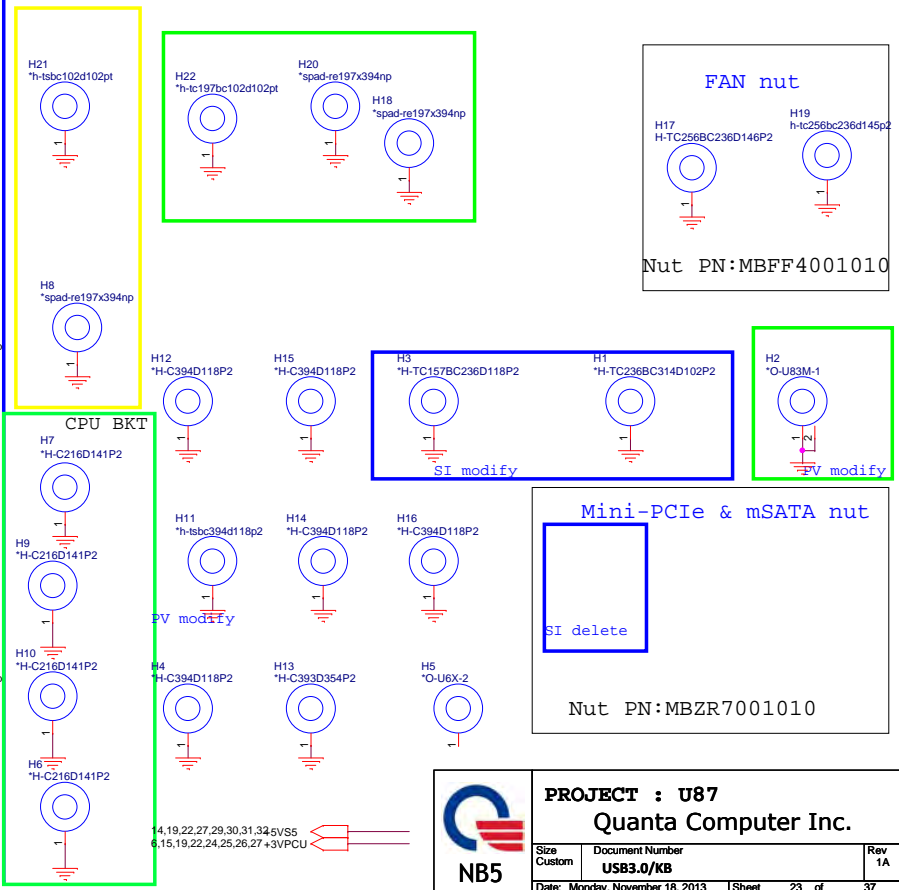
KEYBOARD PULL-UP



USB 2.0/3.0 Combo



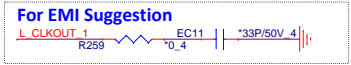
Hole

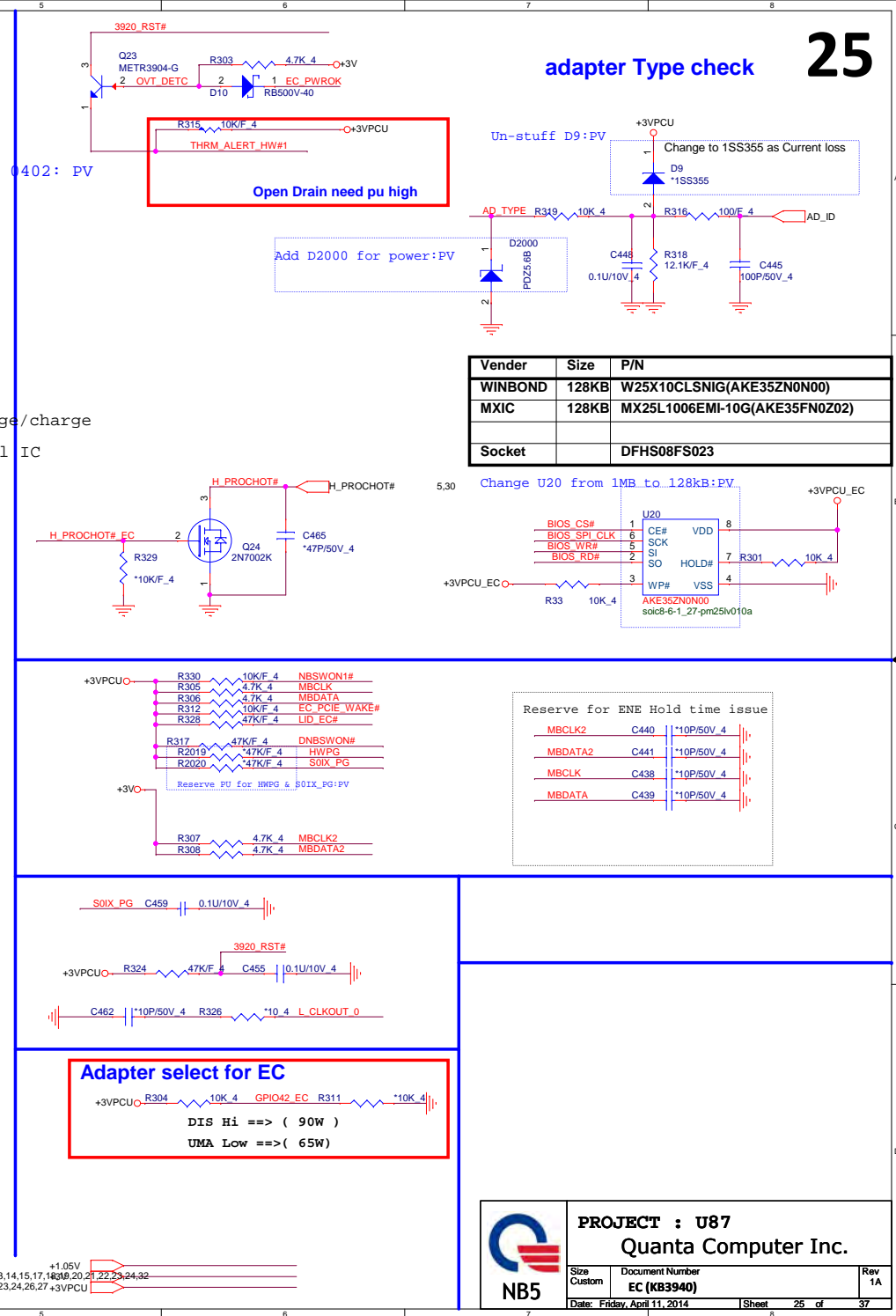


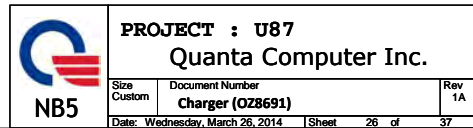
PROJECT : U87
Quanta Computer Inc.

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Custom	USB3.0/KB	1A
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NB5



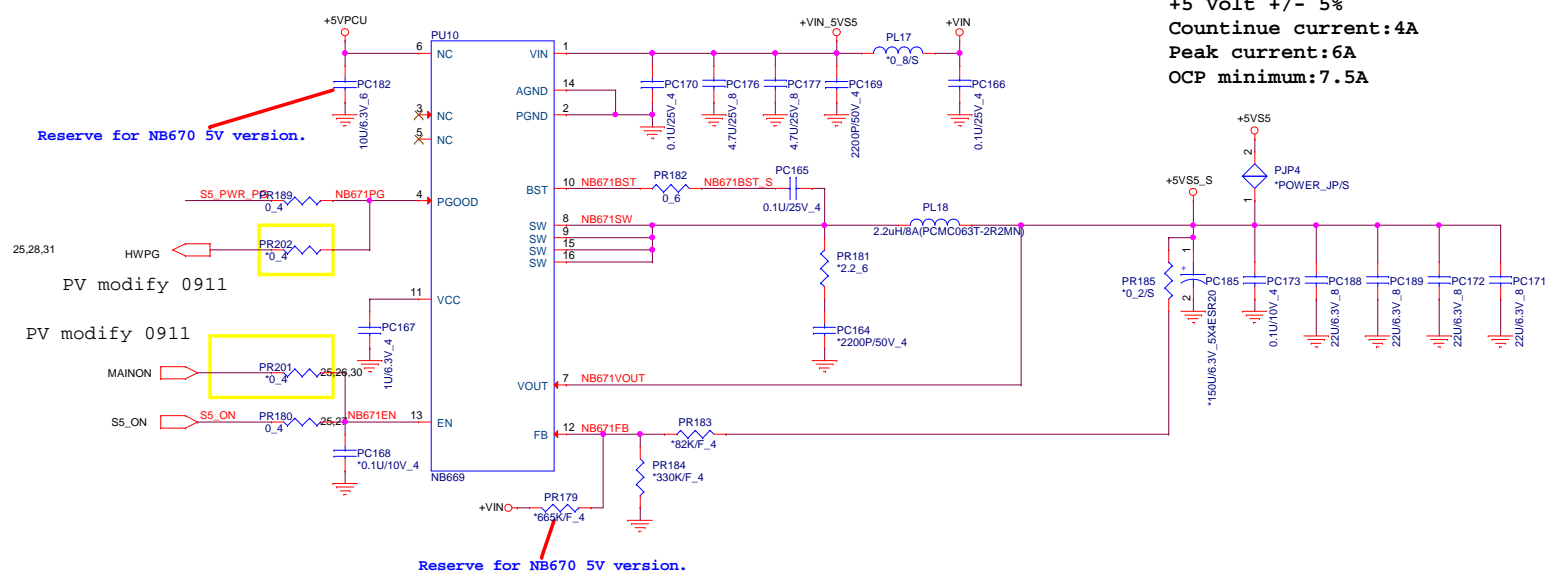




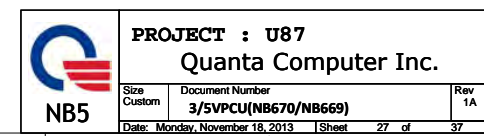
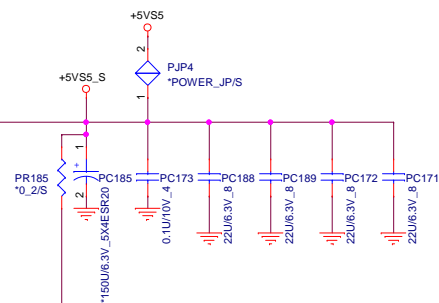


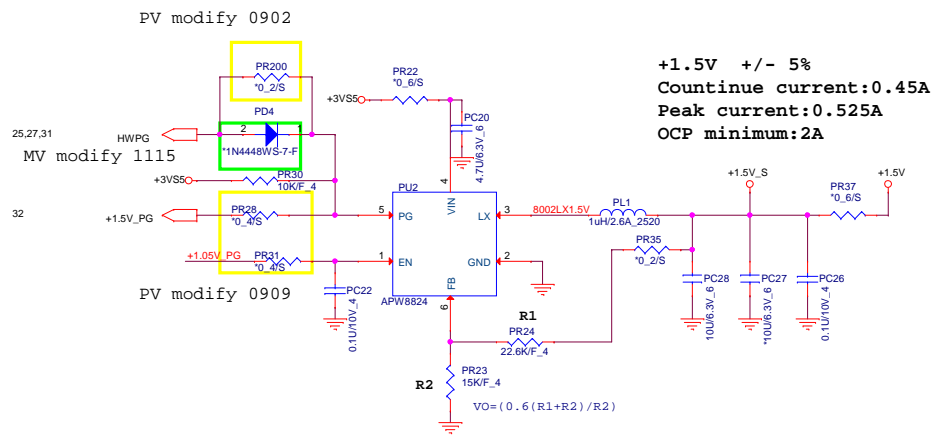
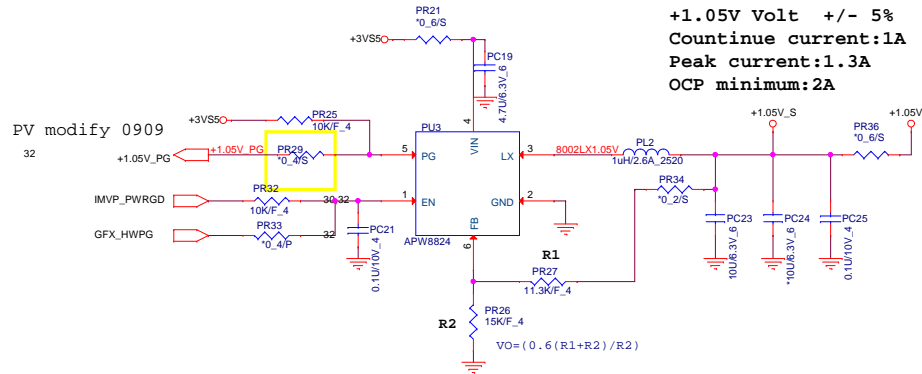
2,9,11,14,15,22,24,28,30,31,32
14,19,22,23,29,30,31,32


+3.3 Volt +/- 5%
Continue current:4A
Peak current:6A
OCP minimum:7.5A

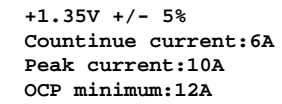


+5 Volt +/- 5%
Continue current:4A
Peak current:6A
OCP minimum:7.5A



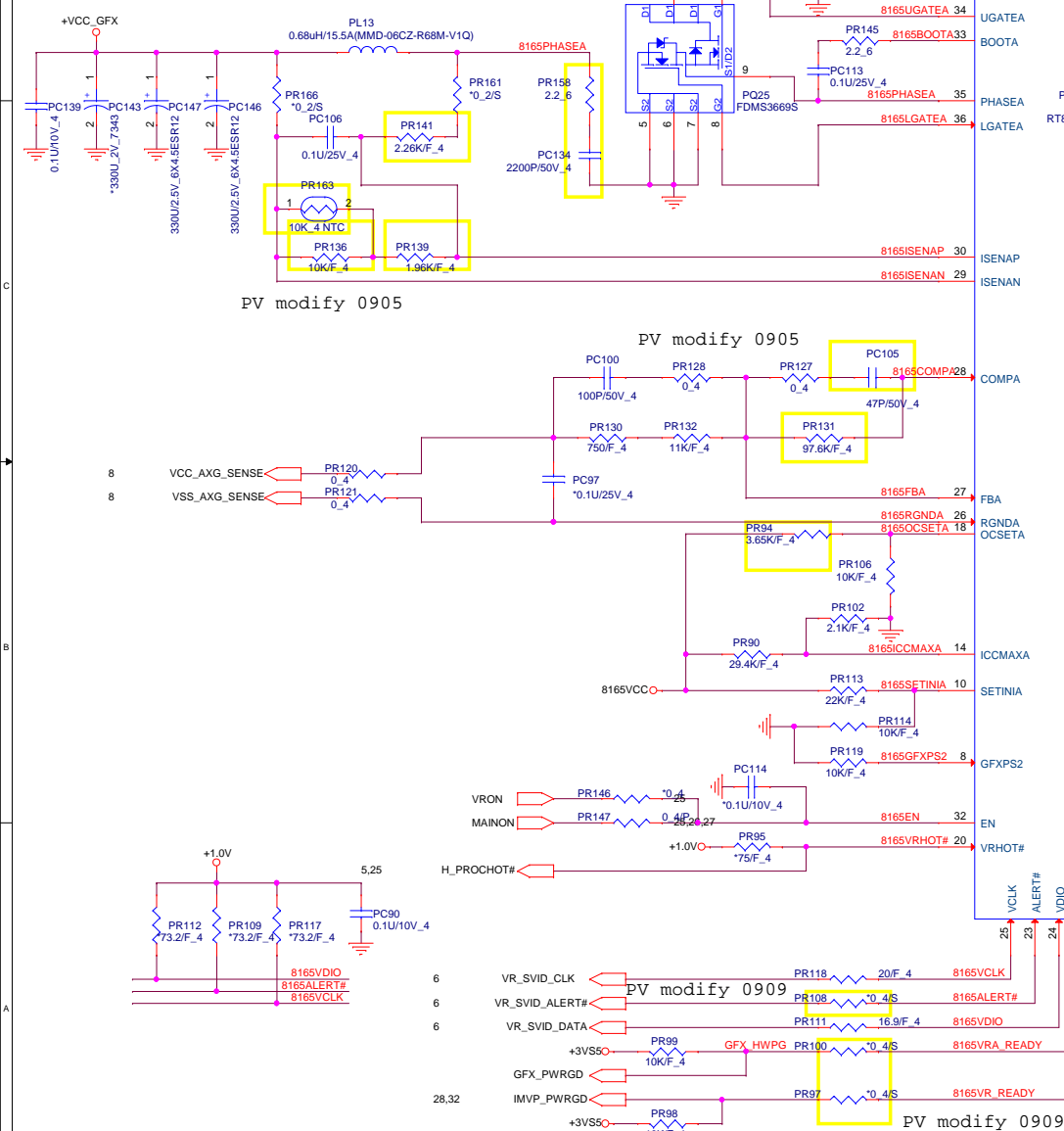


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	Quanta Computer Inc.		
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	+1.05V/+1.5V (SY8002)		
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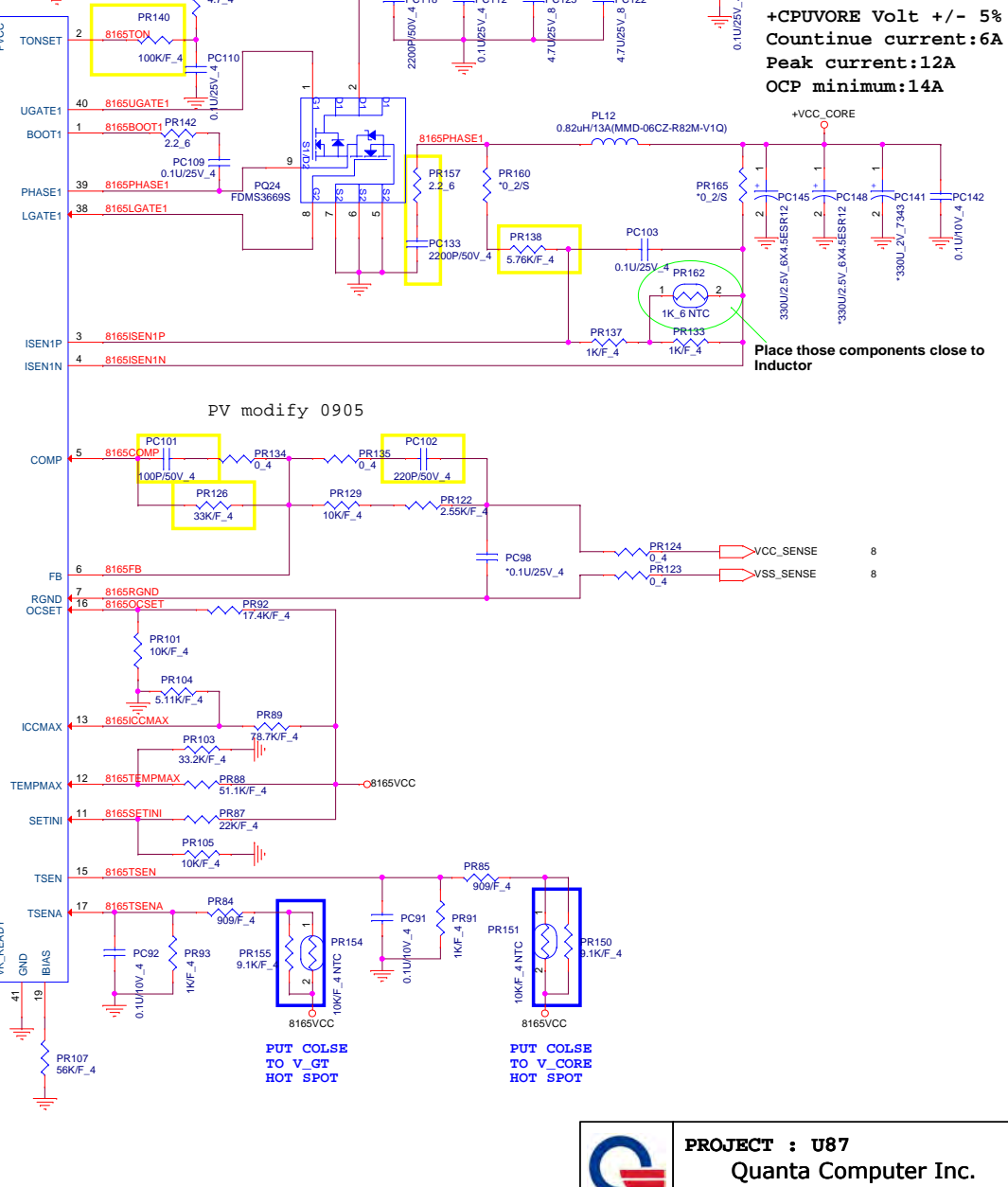


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+GFXORE Volt +/- 5%
Countinue current:6A
Peak current:14A
OCP minimum:16.5A



PV modify 0905

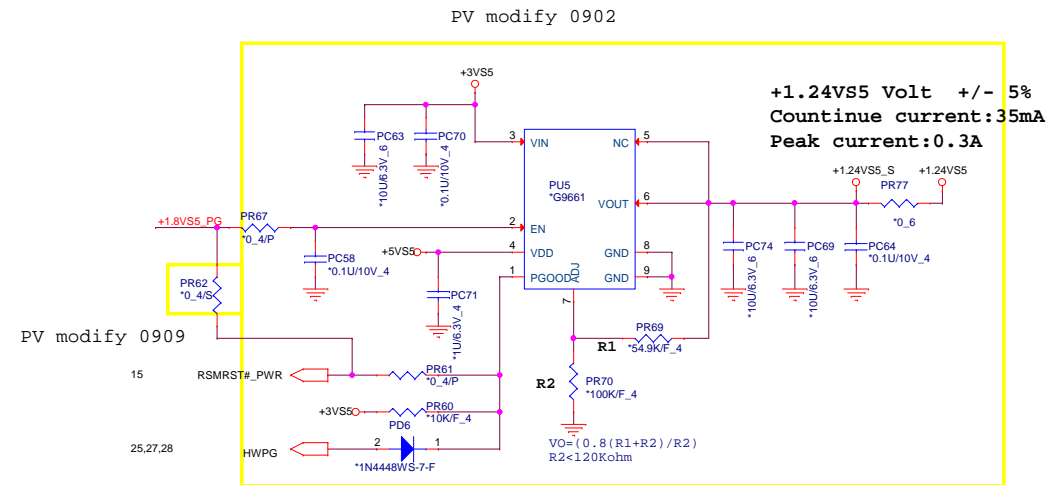
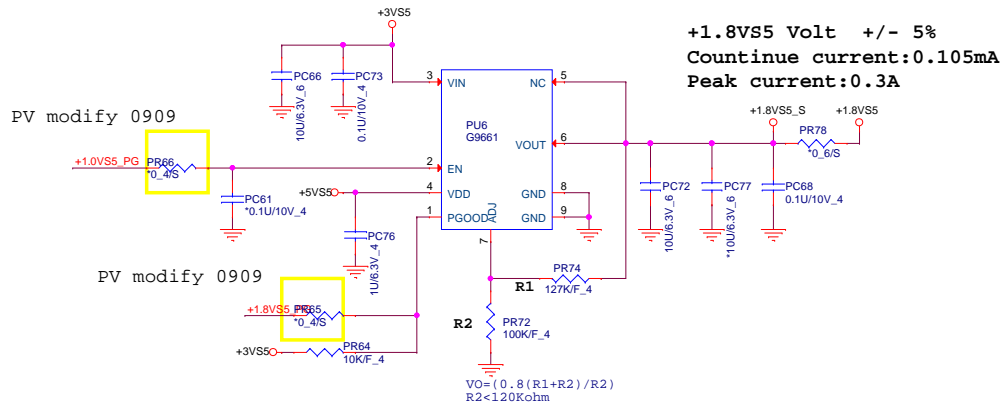
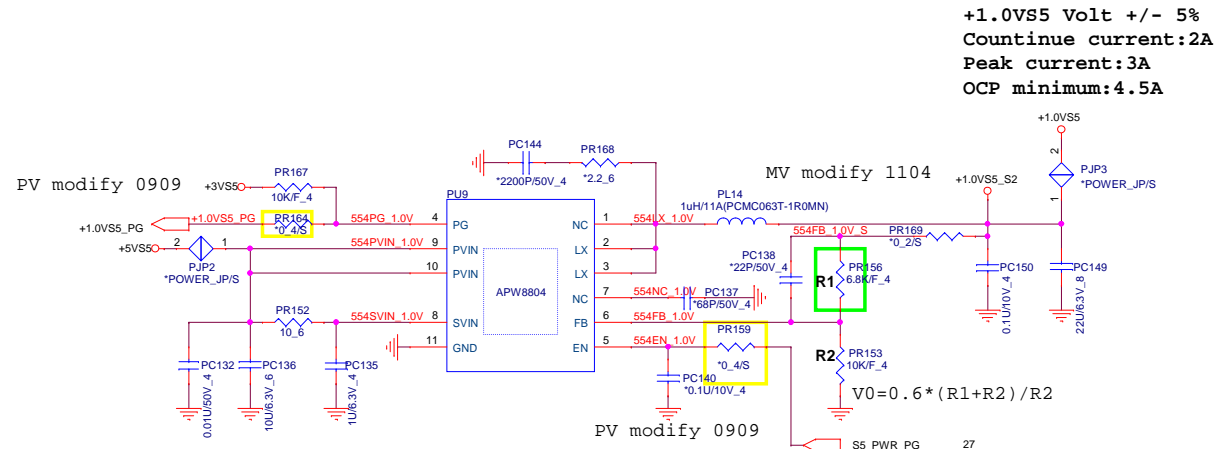


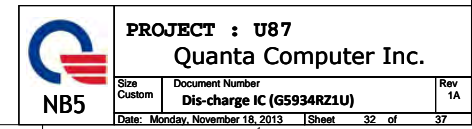
+CPUVORE Volt +/- 5%
Countinue current:6A
Peak current:12A
OCP minimum:14A

Place those components close to Inductor

PUT COLSE TO V_GT HOT SPOT

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Quanta Computer Inc.	
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USB3.0	Port Assignment	Power control pin
PORT0	USB HUB	

USB2.0	Port Assignment	Power control pin
PORT0	USB HUB	N/A
PORT1	Right side USB Daughter BD	USBPW_ON#(from EC)
PORT2	BT	N/A
PORT3	Camera	N/A

USB HUB	Port Assignment	Power control pin
USB30 PORT1	USB2.0/USB3.0 COMBO 1ST	USBPW_ON#(from EC)
USB30 PORT2	USB2.0/USB3.0 COMBO 2nd	USBPW_ON#(from EC)
USB30 PORT3	N/A	
USB30 PORT4	N/A	
USB20 PORT1	USB2.0/USB3.0 COMBO 1ST	USBPW_ON#(from EC)
USB20 PORT2	USB2.0/USB3.0 COMBO 2nd	USBPW_ON#(from EC)
USB20 PORT3	TS	TS_ON
USB20 PORT4		

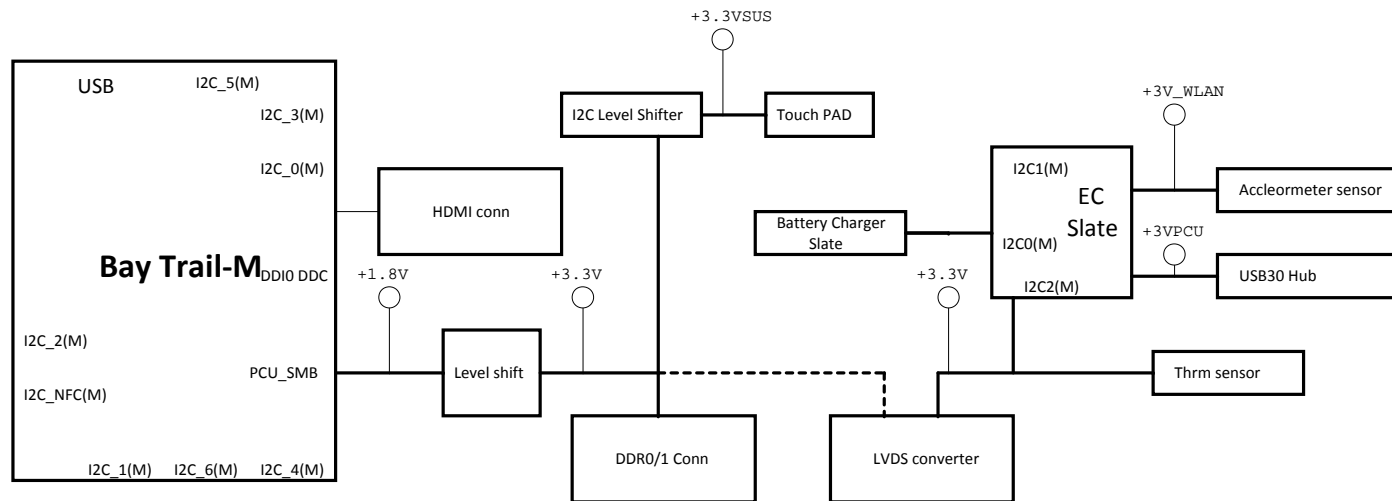
SATA Master	Port Assignment	Power control pin
SATA0	HDD	N/A
SATA1	ODD	ZERO_PWR_ODD

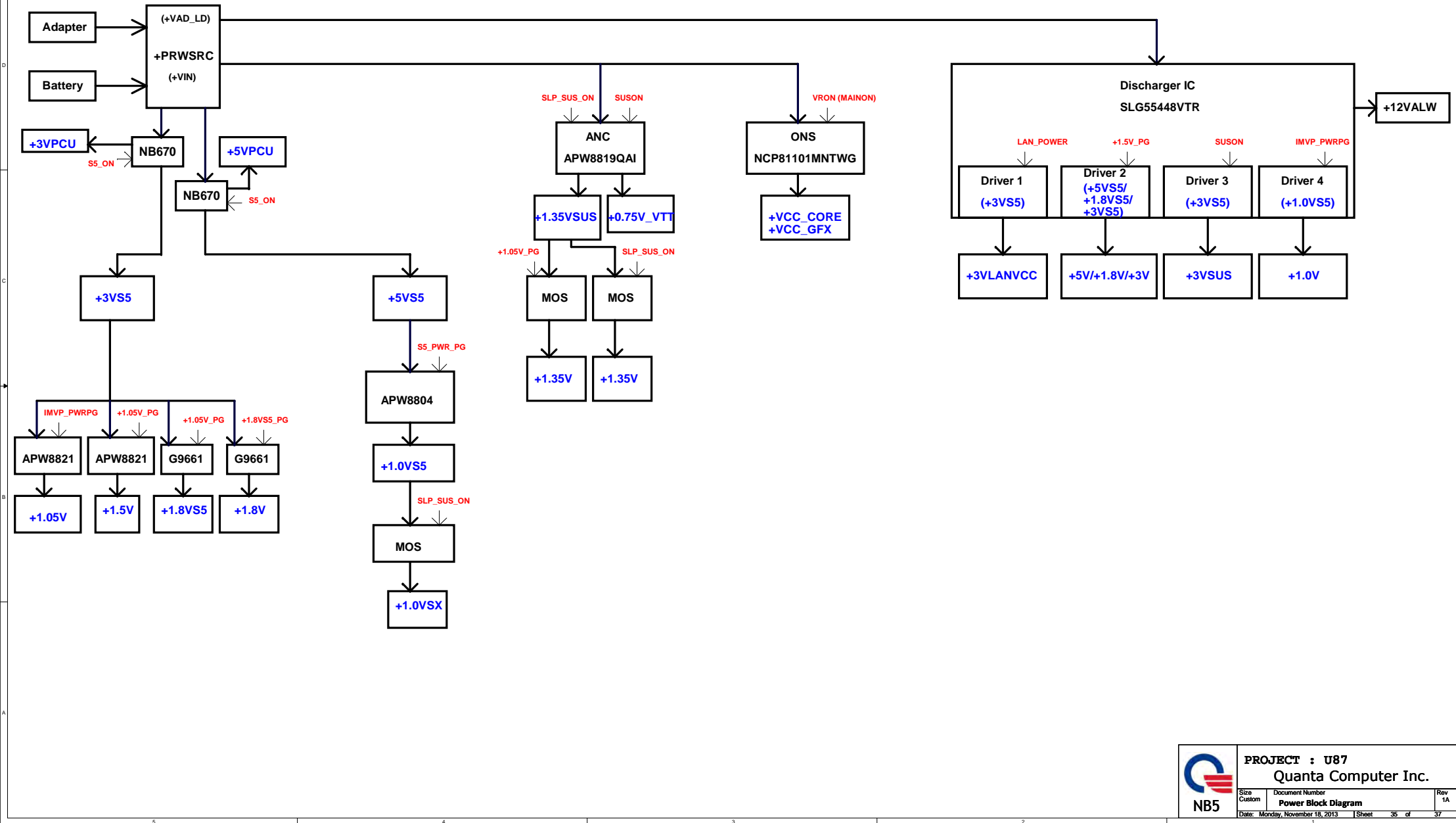
PCIE	Port Assignment	Control pin
PCIE 0	Card reader	
PCIE 1	WLAN	
PCIE 2	LAN	
PCIE 3	NC	

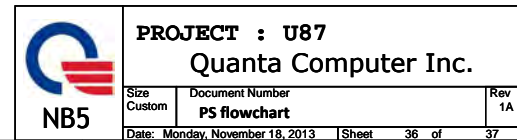



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Quanta Computer Inc.

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